CLAIMS

What is claimed is:

- 1. A method comprising:
 - measuring electrical characteristics of an interconnection; and

determining a test network having electrical characteristics such that the electrical characteristics of the interconnection are approximated by the electrical characteristics of the test network within a specified tolerance.

- 2. The method of claim 1 wherein the test network is a resistive/capacitive network.
- 3. The method of claim 2 wherein measuring includes creating a graphical representation of an output of the interconnection.
- 4. The method of claim 3 wherein determining includes creating a graphical representation of an output of the resistive/capacitive network that approximates the graphical representation of the output of the interconnection within a specified tolerance.
- 5. The method of claim 4 wherein the specified tolerance is 10%.
- 6. The method of claim 1 wherein the test network is a resistive network.
- 7. The method of claim 1 wherein the test network is a capacitive network.

- 8. The method of claim 1 wherein the test network is comprised of a plurality of resistive/capacitive networks.
- 9. The method of claim 2 further including:

 connecting the resistive/capacitive network between a driver of a first input/output circuit and a receiver of a second input/output circuit.
- 10. The method of claim 2 further including: connecting the resistive/capacitive network between a driver of an input/output circuit and a receiver of the input/output circuit.
- 11. The method of claim 10 wherein the resistance and capacitance of the resistive/capacitive network are adjustable.
- 12. The method of claim 11 wherein the resistive/capacitive network is implemented on an integrated circuit chip.
- 13. The method of claim 12 wherein the capacitance is distributed RC ladder.
- 14. The method of claim 11 wherein the resistive/capacitive network is implemented on a printed circuit board.

15. An apparatus comprising:

an integrated circuit having at least one input/output ports, the at least one input/output ports having a driver and a receiver; and

a test network electrically coupling the driver and the receiver such that an input/output interface interconnection may be emulated therewith.

- 16. The apparatus of claim 15 wherein the test network is a resistive/capacitive network.
- 17. The apparatus of claim 15 wherein the test network is a resistive network.
- 18. The apparatus of claim 15 wherein the test network is a capacitive network.
- 19. The apparatus of claim 16 wherein the resistance and capacitance of the resistive/capacitive network are adjustable.
- 20. The apparatus of claim 16 wherein the integrated circuit and the resistive/capacitive network are implemented on a same integrated circuit chip.
- 21. The apparatus of claim 16 wherein the resistive/capacitive network is implemented on a printed circuit board.

- 22. The apparatus of claim 15 wherein the integrated circuit is part of a microprocessor.
- 23. An apparatus comprising:

a test network for an input/output interface having elements selected such that electrical characteristics of the test network approximate electrical characteristics of an input/output interface interconnection within a specified tolerance.

- 24. The apparatus of claim 23 wherein the elements are resistive elements and capacitive elements.
- 25. The apparatus of claim 24 wherein the resistive elements and the capacitive elements are adjustable such that the test network may be used to approximate the electrical characteristics of a plurality of input/output interface interconnections.
- 26. The apparatus of claim 24 wherein the test network is comprised of a plurality of resistive/capacitive networks.
- 27. The apparatus of claim 26 wherein the capacitive elements are distributed RC ladder.
- 28. The apparatus of claim 27 implemented within an integrated circuit chip.
- 29. The apparatus of claim 27 implemented on a printed circuit board.

30. The apparatus of claim 23 wherein the elements are determined such that a graphical representation of an output of the test network approximates, within a specified tolerance, the graphical representation of an output of a particular input/output interface interconnection.